

In the present version, the electronic tongue contains 12 analog cells: nine oxidation/reduction (redox) electrochemical cells, an electrical-conductivity cell, and the aforementioned heater and temperature sensor. The interface circuitry (see figure) consists mainly of 12 digital-to-analog converters (DACs) for excitation of the cells, and four analog-to-digital converters (ADCs) for readout from the cells connected to 12 analog cells. Each analog cell is made of two instrument amplifiers, two operational amplifiers and analog filters for reduc-

ing signal-to-noise ratios, and control and switching circuits.

The interface circuitry resides on a board mounted immediately below the ceramic substrate and, as in the prior version, is connected to the analog cells via miniature edge connectors on the ceramic substrate. By thus placing the ADCs and DACs near the analog cells, the design helps to minimize pickup of noise and reduce cross-talk on the analog signal lines.

As in the prior version, the control circuitry can be programmed to make the DACs generate the specified excitation

waveforms and to make the ADCs acquire the specified response waveform data, and each electrochemical cell can be addressed individually. Depending on the specific application, a given electrochemical cell can be operated in a potentiostatic mode (voltage forced, current measured) or a galvanostatic mode (current forced, voltage measured), or can be made to alternate between the two modes. In one typical application, the main sequence of excitations and responses in a potentiostatic mode is chosen to implement anodic stripping voltammetry or cyclic voltammetry. In another typical application, a working electrode of a cell is operated in a galvanostatic mode at a positive bias for generating oxygen or a negative bias for generating hydrogen.

This work was done by Didier Keymeulen and Martin Buehler of Caltech for NASA's Jet Propulsion Laboratory.

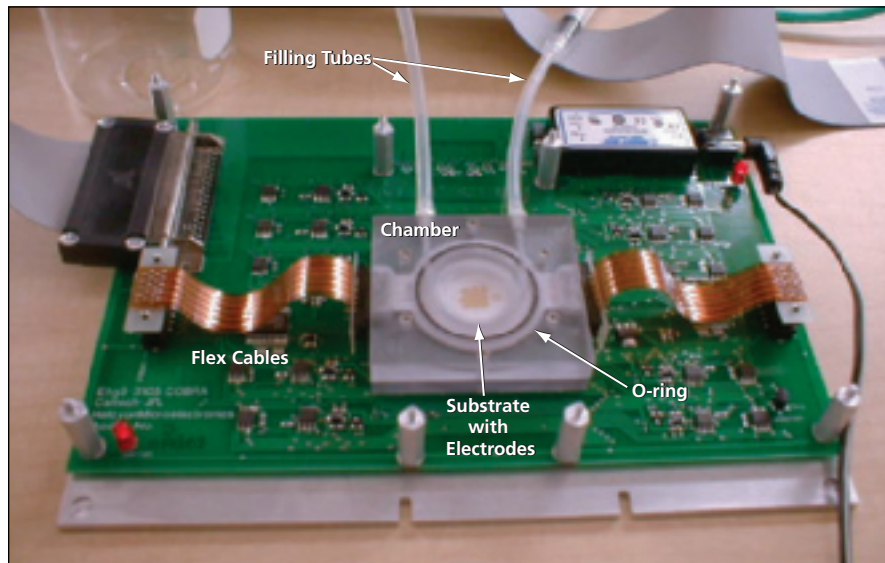
In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

*Innovative Technology Assets Management
JPL*

*Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
(818) 354-2240*

E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-41365, volume and number of this NASA Tech Briefs issue, and the page number.



The **Interface Circuitry** is laid out compactly on a board that, when installed, lies immediately below the electronic tongue.

Inexpensive Clock for Displaying Planetary or Sidereal Time

An external oscillator is substituted for an internal quartz clock oscillator.

NASA's Jet Propulsion Laboratory, Pasadena, California

An inexpensive wall clock has been devised for displaying solar time or sidereal time as it would be perceived on a planet other than the Earth, or for displaying sidereal time on the Earth. The concept of a wall clock synchronized to a period other than the terrestrial mean solar day is not new in itself. What is new here is that the clock is realized through a relatively simple electronic modification of a common battery-powered, quartz-crystal-oscillator-driven wall clock (which, as unmodified, displays terrestrial mean solar time).

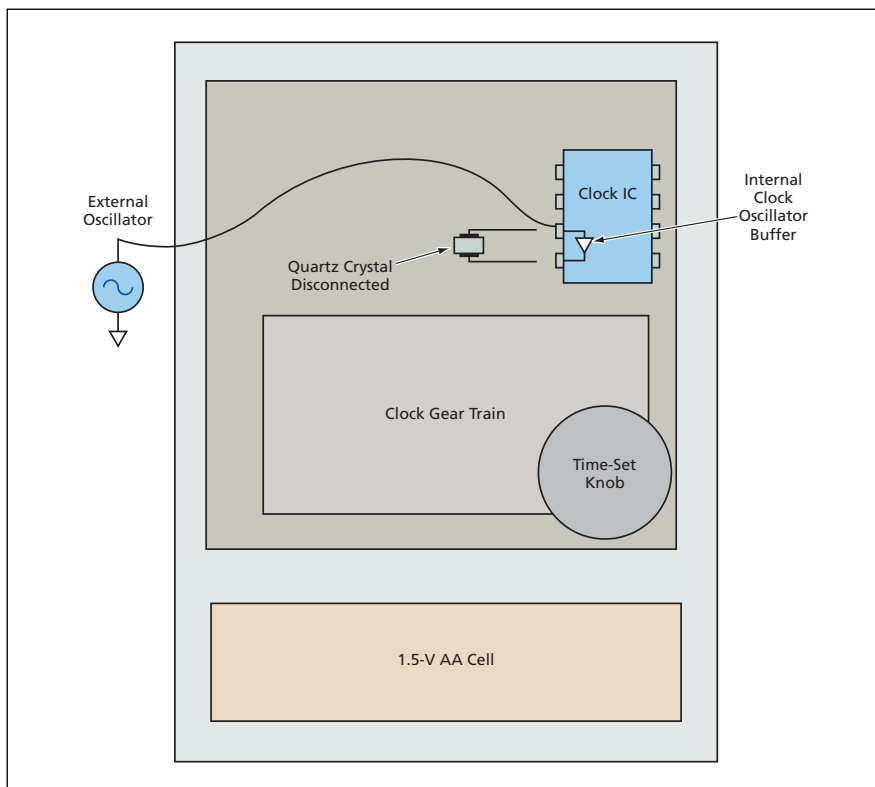
The essence of the modification is to shut off the internal oscillator of the clock and replace the internal-oscillator output signal with a signal of the required frequency generated by an external oscilla-

tor. The unmodified clock electronic circuitry includes a quartz crystal connected to an integrated circuit (IC) that includes, among other parts, a buffer amplifier that conditions the oscillator output. The modification is effected by removing the quartz crystal and connecting the output terminal of the external oscillator, via a capacitor, to the input terminal of the buffer amplifier (see figure).

The frequency and amplitude of the external-oscillator signal must be chosen in accordance with the IC design as well as the desired clock speed. Typically, the required amplitude is 0.5 V peak-to-peak and the frequency required for two complete revolutions of the hour hand (two 12-hour cycles) spanning a terrestrial mean solar day is $2^{15} = 32,768$ Hz. Examples of other clock cycles

and frequencies based on this typical design include the following:

- For one complete revolution of the hour hand (one 24-hour cycle) during a terrestrial mean solar day, the required frequency is $2^{14} = 16,384$ Hz.
- For two complete revolutions of the hour hand (two 12-"hour" cycles) during a terrestrial sidereal day, the required frequency is 32,859.27577 Hz.
- For one complete revolution of the hour hand (one 24-"hour" cycle) during a terrestrial sidereal day, the required frequency is 16,429.63788 Hz.
- For two complete revolutions of the hour hand (two 12-"hour" cycles) during a Martian mean solar day, the required frequency is 31,947.1361 Hz.
- For one complete revolution of the



An **External Oscillator Is Substituted** for the internal quartz-crystal oscillator of a common battery-powered wall clock.

hour hand (one 24-“hour” cycle) during a Martial sidereal day, the required frequency is 15,973.568 Hz.

It is worthwhile to note that for the 24-hour or for any of the 24-“hour” clock speeds, the minute hand would complete a revolution in 2 hours or “hours”. Therefore, it could be desirable to remove the minute hand to prevent confusion. In addition, in that case, the 12-hour faceplate must be replaced by a 24-hour faceplate.

It is also worthwhile to note that the precision of the clock display depends on the precision of the external oscillator, which can be cheap or expensive, as needed to obtain the precision required for a specific application. For example, the external oscillator could be a battery-powered, fixed-frequency quartz oscillator; a commercially available programmable integrated-circuit frequency synthesizer; or a programmable frequency synthesizer locked to highly stable reference oscillator (e.g., a hydrogen maser).

This work was done by James Lux of Caltech for NASA’s Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-40845

Efficient Switching Arrangement for $(N + 1)/N$ Redundancy

This arrangement can be generalized beyond its initial application.

NASA’s Jet Propulsion Laboratory, Pasadena, California

An efficient arrangement of four switches has been conceived for coupling, to four output ports, the output powers of any subset of four devices that are members of a redundant set of five devices. In normal operation, the output power of each of four of the devices would be coupled to one of the four output ports. The remaining device would be kept as a spare: normally, its output power would be coupled to a load, wherein that power would be dissipated. In the event of failure of one of the four normally used devices, that device would be disconnected from its output port and connected to the load, and the spare device would be connected to the output from which the failed device was disconnected. Alternatively or in addition, the outputs of one or more devices could be sent to ports other than the ones originally assigned to them.

In the original intended application, the devices would be microwave amplifiers and the switches would be mechan-

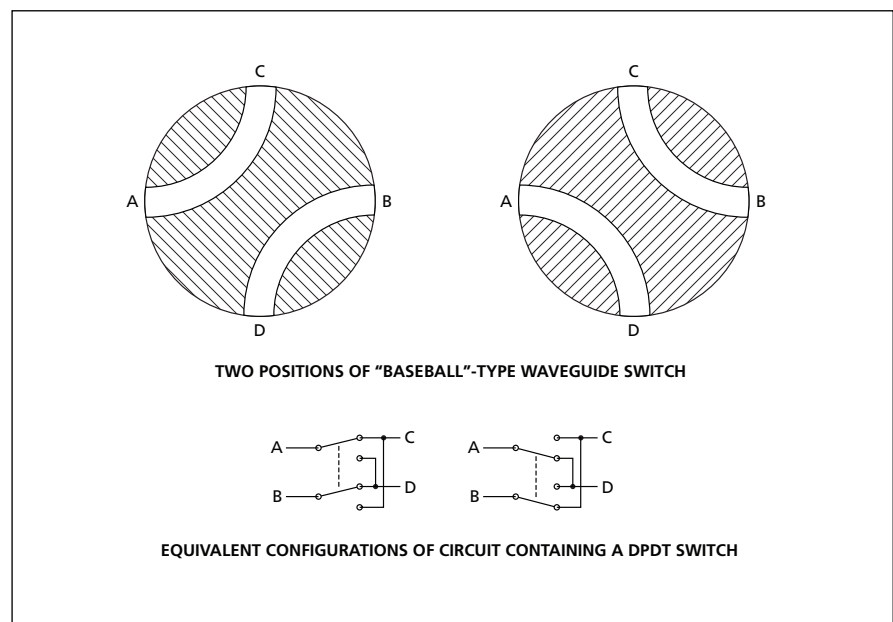


Figure 1. Ports A, B, C, and D can be connected in either of two different combinations of pairs, depending on the setting of a waveguide switch of the “baseball” type. Nominally equivalent switching could be effected by use of an electric circuit containing a DPDT switch.